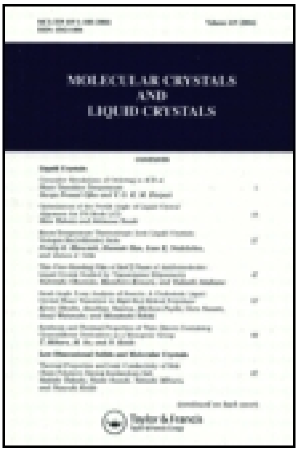

Molecular Crystals and Liquid Crystals
Publication details, including instructions for authors and subscription information:
http://www.tandfonline.com/loi/gmcl20

Three-Dimensional Organic Field-Effect Transistors Using Solution-Processed Thin Films of Benzothieno-Benzothiophene Derivatives

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Version of record first published: 16 May 2011

Mol. Cryst. Liq. Cryst., Vol. 539: pp. 58/[398]–62/[402], 2011

ISSN: 1542-1406 print/1563-5287 online
DOI: 10.1080/15421406.2011.566055

Three-Dimensional Organic Field-Effect Transistors Using Solution-Processed Thin Films of Benzothieno-Benzothiophene Derivatives

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Organic field-effect transistors utilizing solution-processed benzothieno-benzothiophene is developed using a three-dimensional field-effect transistor structure, which comprises multiple vertical channels to enhance their output drain current. The soluble benzothieno-benzothiophene thin films were formed on vertical channels using different solvents, and the mobility is estimated to be 3.7×10^{-3} cm^2/Vs. Nevertheless, extremely large values of channel width divided by length enables current amplification up to 0.7 mA per device area of 1 cm^2, even with the low carrier mobility. The result demonstrates the usefulness of the three-dimensional structure to produce high output currents for device applications.

Keywords Organic field-effect transistor; organic semiconductor; solution process; three-dimensional transistor; vertical transistor

1. Introduction

Since organic thin-film transistors (OTFTs) and organic light emitting devices have many advantages in terms of simplicityity and low-cost, low-temperature process, and compatibility with flexible substrates, they are promising for future flexible and light-weight device applications, so that such products as flexible displays become practical [1]. One of the most attractive features of some classes of organic semiconductor materials is their solubility and easiness to form crystalline films using very simple fabrication processes such as drop-casting and spin-coating [2,3]. Recently, very high field-effect mobility exceeding 1 cm^2/Vs was reported for solution-processed organic field-effect transistors (OFETs) of 2,7-dialkyl[1]benzothieno[3,2-*b*][1]benzothiophenes (C_n-BTBT: $n = 8$–12) [4], whose molecular structure is shown in Figure 1. C_n-BTBT, are attractive materials used in

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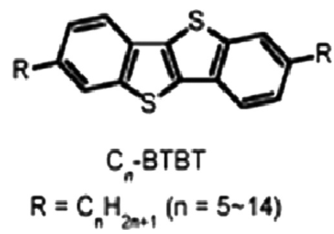

Figure 1. Chemical structure of C_n-BTBT.

solution-processed OTFTs because of their high mobility and good stability in air [4]. Furthermore, T. Uemura *et al.* have developed a method of fabricating highly crystallized films from the solution, holding the solvent liquid at the edge of a sustaining piece. The maximum mobility of C_8-BTBT reached 5 cm^2/Vs [5], which is the best performance realized in solution-processed organic semiconductor films.

In this study, C_8-BTBT thin films are formed by the solution process using three dimensional organic field-effect transistors (3D-OFETs) structures [6,7]. The 3D-OFETs are comprised of multiplied vertical channels, all of which are electrically connected, so that they can yield high output current from the multiplied channels, essentially elevating the space availability. One of the advantages to adopt the 3D structure is that the channels are less deformed even when the substrates are bent, because the channels are vertically built to the substrates. The present authors have previously reported that 3D-OFETs with vacuum-deposited dinaphthothieno [3,2-b]thiophenes (DNTT) [8] films showed an unprecedented high output current density exceeding 10 A/cm^2 with an on/off ratio of 10^5, and a fast switching speed within 0.2 μs [6]. The present study focused on fabricating the organic semiconductor in 3D-OFETs by solution process. It is demonstrated that the simple solution process is applicable to form organic films on the vertical sidewalls of 3D-OFETs.

2. Experiment

Figure 2 shows a schematic structure of the 3D-OFET. Semiconductor channels are built on the sidewalls of the 3D structure, so that injected carriers flow vertically from the source electrode at the groove part to the drain electrode on the land part of the structure. Since the channel width W corresponds to the total length of all the vertically structure edges and the channel length L equals to

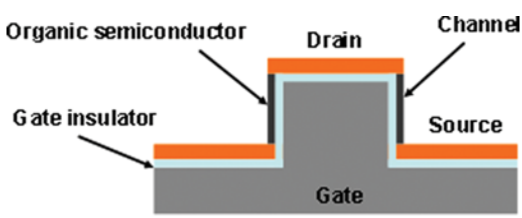

Figure 2. Schematic illustration of the 3D-OFET.

the height of the structures, one can design the device with a large ratio of W/L. The output drain current I_D can be expressed using the field-effect mobility μ and the channel ratio W/L as:

$$I_D = \mu c_i \frac{W}{L} (V_G - V_{th}) V_D,$$

where c_i is the gate capacitance per channel area, and V_G, V_{th}, and V_D are the gate voltage, the threshold voltage, and the drain voltage, respectively. Since the 3D structure has large W/L ratio, a drain current becomes very high, even when the carrier mobility is low. The fabrication process is shown in Figure 3. To fabricate the micro-columns on Si substrates, photolithography technique was used. First, photo-resist pattern was fabricated on a Si substrate, and Si was dry-etched normal to the substrate. Etching depths are varied from 1.7 μm to 20 μm. After peeling off the photo-resist, 500-nm-thick SiO_2 layer is thermally grown on the Si substrate. For source and drain electrodes, gold films of 20 nm thick were deposited by resistively-heated vacuum depositions from strict upright direction to the structure. Then, the gold electrodes are treated with pentafluorobenzenethiol (PFBT) to reduce the surface free energy on them, and to suppress the solution to be held on the electrodes. Finally, saturated solutions of C_8-BTBT with solvent heptane, tetrahydrofuran (THF), and 2,4-trichlorobenzene (TCB) are prepared at room temperature, and casted onto the micro-structures and air-dried for more than 6 hr. The widths and the pitches of the columns are varied from 5 to 20 μm, and the heights of the columns are varied from 1.5 to 20 μm. The W/L ratio of the vertical channels are from 500 to 10000, in a total device area of typically $510 \times 510\,\mu m^2$. FET characteristics of the devices were measured in ambient condition using a semiconductor parameter analyzer (Agilent B1500A).

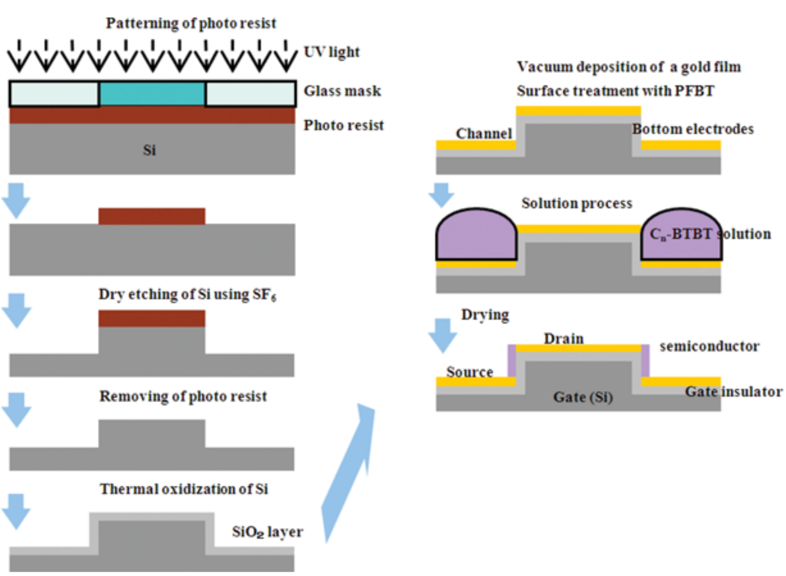

Figure 3. Fabrication process of the 3D-OFET.

3. Results and Discussion

Figure 4(a), 4(b), and 4(c) show the scanning electron microscopy (SEM) images of the fabricated 3D-OFETs before casting of solution. Figure 4(b) and 4(c) show the expanded views of the channels with the channel lengths of 10 μm and 1.7 μm, respectively. Since the sidewalls of the structures are highly perpendicular to the substrate, the gold films deposited at the land part and the groove part of the structure were separated electrically, which enabled fabrication of both source and drain electrodes in the single process.

Figure 5 shows the typical FET characteristics of one of the prepared devices from heptane solution with the channel length of 12 μm. The channel width W are calculated to be 13770 μm, so the channel ratio of W/L is calculated to be 1148 per $510 \times 510\,\mu m^2$ area. Figure 5(a) shows the output characteristics, and Figure 5(b) is the transfer characteristics of the same device in the linear regime. The carrier mobility on the vertical channels is estimated to be $2.6 \times 10^{-3}\,cm^2/Vs$ in the linear regime. The domain sizes of the device are observed to be more than 20 μm on the groove part. We note that the coverage ratio of the crystalline films to the total area of sidewalls are about 40%, which means that the area of actually-working semiconductor channels are less than the intended value. The statistics of the measured field-effect mobility are all in the range from 1.2×10^{-3} to $3.7 \times 10^{-3}\,cm^2/Vs$ for the other six samples. The devices fabricated using TCB solutions showed carrier mobilities at $10^{-5}\,cm^2/Vs$ range. In TCB case, large-size domains appeared on top of the vertical structures. The devices fabricated from THF solutions did not show FET operations. The values much smaller than that

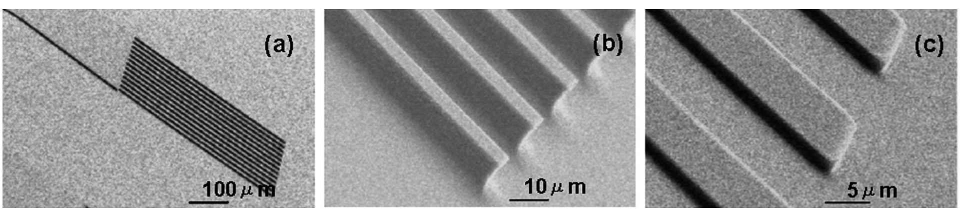

Figure 4. SEM images of vertical channels (a) before casting of solution, and expanded pictures with the channel lengths of (b) 10 μm and (c) 1.7 μm.

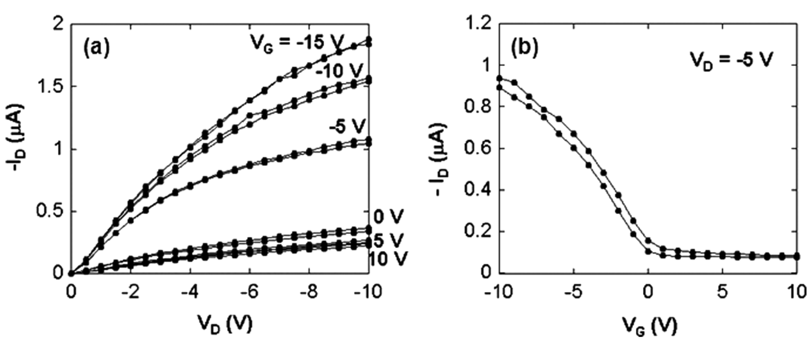

Figure 5. FET characteristics of C_8-BTBT. (a) output characteristics, (b) transfer characteristics at $V_D = -5\,V$.

obtained for lateral devices suggest that the quality of the thin films in the present vertical channels has not been optimized yet. To achieve higher mobility, it would be necessary to further improve casting conditions so that the whole surface of the sidewalls are covered without weak links. Nevertheless, the field-induced current reaches 1.8 μA ($V_D = -10$ V, $V_G = -15$ V), which corresponds to the output current density of about 0.7 mA/cm^2. The present combinations of the huge W/L ratio of more than 10^3 and rather low mobility of $10^{-3}\,cm^2/Vs$ corresponds to the configurations of W/L ratio of 1 and carrier mobility of 4.6 cm^2/Vs in planar TFTs, from a point of view of obtaining high output current of TFTs. The result provides an alternative solution to realize high mobility, suggesting a promising perspective for the technology of the full-organic displays incorporating OLEDs and the 3D OFETs.

In summary, 3D-OFETs are more advantageous in producing high output current than conventional plane OFETs, due to their high ratio of W/L. C_8-BTBT thin films are formed on the vertical channels using a simple solution process, and the mobilities of $4 \times 10^{-3}\,cm^2/Vs$ are obtained. It is proven that the simple solution process is applicable to form the organic semiconductor on 3D structure, and suggests a potential to achieve high performance with solution-processed 3D-OFETs, which can be applied to such devices as matrix controlling elements in flexible displays.

Acknowledgment

This study is supported by NEDO's Research and Development of Nanodevices for Practical Utilization of Nanotechnology (Nanotech Challenge Program) (2009), Japan.

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